AMENDMENTS TO THE CLAIMS

130. An integrated circuit device comprising:

a circuit to convert an input value into a search value;

a first storage including content addressable memory (CAM) cells, compare lines coupled to columns of the CAM cells and match lines coupled to rows of the CAM cells, the compare lines being coupled to receive the search value;

a second storage coupled to the match lines of the first storage; and

a compare circuit coupled to an output of the second storage and coupled to receive the input value.

131. The integrated circuit device of claim 130 wherein the second storage comprises an array of static random access memory (SRAM) cells.

132. The integrated circuit device of claim 130 wherein the second storage comprises an array of dynamic random access memory (DRAM) cells.

133. The integrated circuit device of claim 130 wherein each of the CAM cells comprises a compare circuit coupled to at least one of the compare lines and at least one of the match lines.

134. The integrated circuit device of claim 130 wherein the CAM cells within a column of the CAM cells comprise respective compare circuits coupled to a common pair of compare lines and to respective match lines.

135. The integrated circuit device of claim 130 wherein the first storage further includes

word lines coupled to the rows of the CAM cells.

136. The integrated circuit device of claim 130 further comprising a select circuit having a first input port coupled to the word lines and a second input port coupled to the match lines.

137. The integrated circuit device of claim 136 wherein the second storage comprises word lines coupled to an output of the select circuit.

138. The integrated circuit device of claim 137 wherein the select circuit is responsive to an operation select signal to select either a decoded row address present on the word lines of the first storage or match signals present on the match lines of the first storage to be output onto the word lines of the second storage.

139. The integrated circuit device of claim 130 wherein the circuit to convert the input value into a search value is a cyclic redundancy check (CRC) circuit that generates a CRC value based on the input value, and wherein at least a portion of the CRC value constitutes the search value.

140. The integrated circuit device of claim 130 further comprising an interface and an assembler circuit coupled to the interface, the assembler circuit being configured to reorder selected bits within a value received via the interface to generate the input value.

141. The integrated circuit device of claim 130 wherein the circuit to convert the input value comprises a mask circuit to mask selected bits in the input value.

142. A content addressable memory (CAM) comprising:

a cyclic redundancy check (CRC) circuit to generate a CRC value; and

a CAM array having compare lines coupled to the CRC circuit to receive at least a portion of the CRC value therefrom.

143. The CAM of claim 142 wherein the CAM further comprises a mask circuit to mask selected bits in the CRC value.

144. The CAM of claim 143 further comprising a configuration circuit to store a configuration value indicative of the selected bits to be masked within the CRC value, the configuration circuit being coupled to the mask circuit to provide the configuration value thereto.

145. The CAM of claim 142 wherein the CRC value comprises N constituent bits and wherein the at least a portion of the CRC value comprises M contiguous bits of the CRC value, M being less than N.

146. A content addressable memory comprising:

a CAM array including a plurality of CAM cells and a plurality of match lines coupled to respective rows of the CAM cells;

a priority index table including a plurality of priority storage circuits coupled to store respective priority values and coupled respectively to the plurality of match lines; and

a multiplexer having a first input coupled to receive a selected priority value from

the priority index table, and a second input to receive a predetermined priority value.

147. The CAM of claim 146 wherein the priority values indicate relative priorities of values stored within corresponding rows of the CAM cells.

148. The CAM of claim 146 wherein the multiplexer is responsive to a select signal to output either the selected priority value or the predetermined priority value.

149. The CAM of claim 146 wherein the multiplexer is configured to output the predetermined priority value in response to an operation to determine whether the CAM is able to store a first value, and wherein the multiplexer is configured to output the selected priority value in response to an operation to determine whether a specified value is stored within the CAM.

150. An integrated circuit device comprising:

means for converting an input value into a search value;

a first storage including means for generating a plurality of match signals that indicate whether the search value matches respective values stored within the first storage;

a second storage including means for outputting a value stored at a location within the second storage indicated by the plurality of match signals; and

means for comparing the value output from the second storage with the input value.